REMARKS

With Claims 1-15 were pending, Claims 5-6 have been cancelled and new Claims 16-22 have been added. Accordingly Claims 1-4 and 7-22 remain for the Examiner's consideration. Claims 1, 8, 10 and 13 have been amended as discussed to follow.

Claims 1-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,100,715 (hereinafter referred to as "Agrawal") in view of U.S. Patent 6,510,530 (hereinafter referred to as "Wu"). Based on the above amendments, and the following remarks, this rejection is respectfully traversed.

Claim 1, as amended, includes a time multiplexing signal generator coupled to the selection device and the capture devices via one time multiplexing signal. As supported by the specification, a time multiplexing signal 401 controls capture devices shown as flip-flops 407 and 410 in Fig. 4A, as well as the selection device 404. [Spec., paras. 0033 and 0034]. During a first phase in which TM signal 401 is in a first logic state, TM signal 401 can select an output signal from source 403A via selection device 404 to be latched by flip-flop 407. During a second phase in which TM signal 401 is a second logic state, TM signal 401 can select an output signal from source 403B (also via selection device 404) to be latched by flip-flop 410. [Spec., para. 0034].

Wu, on the other hand, discloses the use of two clocks with different frequencies driving its capture devices, or latches 17 and 19. Clocks f_0 and f_1 are used by output latches 17 and 19, respectively, to provide the data output for the respective ports p0 and p1 of the CsRAM 10. [Fig. 1A and col. 4, lines 6-11]. Wu neither discloses nor suggests one clock for use by both latches 17 and 19. Therefore, Wu does not disclose a single time multiplexing clock signal that coordinates latching of a source signal in corresponding capture devices, as required by Claim 1.

Agrawal does not further disclose capture devices as controlled by a single clock. Agrawal discloses a dedicated multiplexer for driving a shared interconnect line in the background section of the patent [col. 2, lines 66-67], and does not further disclose capture devices coupled with a time multiplexing signal generator as claimed.

Claim 1 is, thus, believed non-obvious in view of the cited references, and reconsideration thereof is respectfully requested.

Claims 2-5 and 7-9 being dependent upon Claim 1 should be allowable for at least the reasons Claim 1 is allowable.

Claim 10 has been amended to recite that a first one of the signals is latched to a first one of the capture devices during a first phase of the time multiplexing signal and a second one of the signals is latched to a second one of the capture devices during a second phase of the time multiplexing signal [See, spec., paras. 0034-0035, and Fig. 4A]. As shown in Fig. 4A of the applicant's specification, the diamond on the time multiplexing signal inputs to capture devices 407 and 410 indicates a complementary inversion controlled by a configuration memory cell. For example, capture device 407 could use a non-inverted signal, as shown by the open diamond, whereas capture device 410 could use an inverted signal, as shown by the filled diamond. Wu, however, does not disclose inverting of clock signals received by the latches 17 and 19. Only buffering is performed on the clock signals from internal clock generator through buffers 18, 23 or 11 and 13 to latches 17 and 19 in Fig. 1A. As mentioned above, Agrawal neither discloses nor suggests the use of latches. For at least these reasons, Claim 10 is believed non-obvious in view of the cited references, and should be allowable.

Further, Claim 10 requires routing signals from the shared programmable interconnect to the capture devices through a first programmable interconnect point. Wu does not disclose a shared programmable interconnect as discussed above for Claim 1 and therefore does not disclose a programmable interconnect point, as required by Claim 10. Agrawal discloses a shared interconnect line in the background section of patent, but there is no discussion regarding whether the shared interconnect line is programmable, as required by Claim 10.

Claims 11-12 being dependent upon Claim 10 should be allowable for at least the reasons Claim 10 is allowable.

Claim 13 as amended includes a multiplexer which chooses between source signals to drive a shared programmable interconnect on the programmable logic

device and a clock which is coupled to the multiplexer and flip flops and provides a signal from the multiplexer to the flip flops without a clock delay. Wu discloses the sRAM memory cell 15 that provides a clock delay in a path between multiplexers 14, 16 and 18 and the latches 17 and 19. Agrawal does not disclose a path from its multiplexer to latches. Accordingly, Claim 13 is believed non-obvious in view of the cited references, and reconsideration thereof is respectfully requested.

Claims 14-15 being dependent upon Claim 13 should be allowable for at least the reasons Claim 13 is allowable.

New Claims 16-22 are believed allowable based at least on their dependency on respective ones of Claim 1 and 13.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 10, 2006.

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